AMENDMENTS TO THE SPECIFICATIONS

On page 1, line 3, please add the following new paragraph:

- -This application claims the benefit under 35 U.S.C. § 365 of European patent application No. 03290401.3 filed February 18, 2003.- -

Please replace the paragraph beginning on page 17, line 29 with the following rewritten paragraph:

- -At the camera 1, a digital demodulating circuit 14 receives the control information sent by modulating circuit 25 and supplies the phase difference value $\Delta\Phi L$ obtained by converting circuit 24 to a digital loop filter 15. Based on this input, the loop filter 15 calculates a control voltage which is supplied to a voltage controlled oscillator 12a via a DAC 17. Another kind of implementation could use a Direct Digital Synthesizer and a free running clock generator, the digital output of the loop filter being applied to the DDS control without D to A conversion. The control voltage defines the frequency of pixel clock PC_C delivered by oscillator 12a to counters 12b, 12c of time base 12. The phase comparator 23, loop filter 15 and oscillator ~~16~~ 12a thus form a phase lock loop for controlling the pixel clock frequency PC_C of camera 1. Since phase lock loops as such and their operation is generally known in the art, the operation of this phase lock loop will not be further described in detail. For the purpose of the present invention, it is sufficient to realize that according to the sign of the phase difference $\Delta\Phi L$ detected by phase comparator 23, the pixel frequency of oscillator 12a will be increased or decreased until the line synchronisation impulses of the video signal from the camera 1 and the local video signal of the mixer are found to be perfectly aligned. - -

Please replace the paragraph beginning on page 19, line 30 with the following rewritten paragraph:

- - In the camera 1, the imager chip 11, time base 12, demodulating circuit 14, loop filter 15, (voltage controlled oscillator ~~16~~ 12a and DAC 17) or (DDS) and reset circuit 18 are the same as in Fig. 1 and need not be described again. The

video signal generating circuit 13 may be slightly different from that of Fig. 1 in that it does not convert the pixel data received from imager chip 11 into an analogue video signal but provides a train of digital data comprising image information and image synchronisation information and supplies it to a data compression circuit 51 of a sending interface 5 inserted between the camera 1 and the downlink transmission line 3. The output of data compression circuit 51 is connected to a FIFO buffer 52 in which the compressed video data stream are temporarily stored before being handed on to a packet forming circuit 53 which groups the data into packets having a format suitable for transmission on the downlink transmission line 3. Also not shown on this block diagram for sake of simplification, a digital modulation circuit and RF up converter may be inserted between the output of circuit 53 and the transmission media. This is especially true in case of radio transmission. - -